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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/602,883	06/26/00	HAAS	A 1-14915

EXAMINER	
NELSON, A	
ART UNIT	PAPER NUMBER
2675	4

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DATE MAILED: 06/20/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/602,883	Haas
Examiner	**Art Unit**
Alecia Nelson	2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jun 26, 2000* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-9, 11-22, 24-34, 37-47, and 50-53* is/are rejected.

7) ☒ Claim(s) *10, 23, 35, 36, 48, and 49* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
18) ☐ Interview Summary (PTO-413) Paper No(s). _____
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1-7, 11-13, 15-20, 25-30, 34, 37-43, 47, and 50-53*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. (U.S. Patent No. 5,307,084) in view of Tanaka (U.S. Patent No. 5,438,290).

With reference to **claims 1-3, 11-13, 15-17, 20, 24-27, 34, 37-43, and 50-53** Yamaguchi et al. teaches data electrodes X_1~X_n and scan electrodes Y_1~Y_n form a matrix configuration for a liquid crystal display panel (3), and are connected to a data driver (1) and scan driver (2). A cell located at an intersection of a scan and data electrode becomes ON-STATE by application of the cell voltages onto the crossing two electrodes, and becomes OFF-STATE by application of the unselective cell voltages there to. A display controller (15), outputs a data driver (1) and X data display signal (XD) to be displayed on the liquid crystal panel (3) in response to an instruction given from a main controller (19). The X data to be displayed on the scan electrodes is serially input from the display controller (15) and is once latched in a shift-register provided in the data

driver (1) and is output in parallel form in synchronization with the selection of a scan electrode Y_i on which the X data XD_i is to be displayed. Logic converting circuit (6) converts an ON-STATE signal and OFF-STATE signal each in the X data XD_i. A line memory (7) composed of a shift register has received and is now storing X data XD_{i-1}' displayed on the just previous scan electrode Y_{i-1} output from the logic converting circuit (6) in response to a data synchronizing signal DCLK output from the display controller (15).

Yamaguchi et al. fails to teach signals which are outputted from the logic circuit that will change up/down the next state of the corresponding electrode from the current state of the electrode. Yamaguchi et al. also fails to specifically teach that logic circuits are configured such that the logic circuit control signals substantially simultaneously connect the change up/down driver to the electrodes.

Tanaka teaches a charging up operation (see column 6, line 60-column 7, line 13), a high voltage sustaining operation (see column 7, lines 14-32), a discharging operation (see column 7, line 33-55), and a low voltage sustaining operation (see column 7 line 6-column 8 line 6). Tanaka also teaches that the low power driver circuit (23) is controlled by a control unit (22) which comprises logic circuits (see column 8, lines 33-35). It is also taught that the control unit (22) comprising the logic circuit determines the output timing of the low power driver circuit (23) (see column 10, lines 5-9). This thereby controls the p-channel and n-channel MOS transistors in a substantially simultaneous manner (see column 8, lines 44-65).

With reference to **claims 4, 18, and 28** all that is needed has been explained above with reference to **claims 1, 15, and 25**. Yamaguchi et al. teaches a logic converting circuit (6) that receives a first input from the display controller (15) via an inverter (61) and a second input from the display controller (15) via OR gate (62). Inverter (61) is input with the mode selecting signal DF, and the exclusive OR gate (62) is input with the output of the inverter (61) and the X data X_{Di} (see column 4, lines 48-59). Yamaguchi et al. fails to teach a signal that are outputted from the logic circuit that will change up/down the next state of the corresponding electrode from the current state of the electrode.

Tanaka teaches a charging up operation (see column 6, line 60-column 7, line 13), a high voltage sustaining operation (see column 7, lines 14-32), a discharging operation (see column 7, line 33-55), and a low voltage sustaining operation (see column 7 line 6-column 8 line 6).

With reference to **claims 5-7, 19, 29, and 30** all that is needed as has been explained above with reference to **claims 1, 15, and 25**. Tanaka further teaches that in the high voltage sustaining operation that the high voltage line and the output terminal are connected to each other so that the high voltage V_0 is supplied to the load capacitor which has been charged up to the voltage V_0. As a result, the high voltage V_0 of the capacitor and the output terminal is sustained (see column 7, lines 27-32). Tanaka also teaches with reference to the low voltage sustaining operation that the ground line and the output terminal are connected to each other so that the ground potential or the zero voltage is supplied to the load capacitor which has been discharged

down to the zero voltage. As a result, the zero voltage of the capacitor and the output terminal is sustained (see column 7, line 68- column 8, line 6).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Yamaguchi et al. and Tanaka to produce an integrated circuit that has an extensive low internal resistance for a low power consumption.

3. ***Claims 8, 9, 14, 21, 22, 31-33, and 44-46*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi et al. in view of Tanaka as applied to **claims 1, 8, and 10** above, and further in view of Weber et al. (5,081,400).

With reference to **claims 8, 14, and 21**, Yamaguchi et al. and Tanaka teaches all that is needed as applied to **claims 1, 11, and 15** as explained above. However, Yamaguchi et al. fails to teach the usage of a diode. Tanaka does teach the usage of diodes (D1) and (D2), but fail to teach that they reduce leakage of current.

Weber et al. teaches that ideal diodes (Dc1) and (Dc2) are included to prevent V_1 from dropping below ground and V2 from rising above Vcc. Weber et al. further teaches without the usage of diodes (Dc1) and (Dc2) the voltages across switches (C1) and (C2) and diodes (Cd1) and (Cd2) would be higher than otherwise, which would cause additional energy to be loosed (see column 10, lines 59-64).

With reference to **claims 9, 22, 31-33, and 44-46**, Yamaguchi et al. and Tanaka teaches all that is needed as applied to **claims 1, 15, 25, and 41** as explained above. However,

Yamaguchi et al. fails to teach the usage of inductors. Tanaka does teach the usage of and inductor L1 which is connected in series to a load capacitor C_L through an output terminal OUT for forming the LC resonance circuit to recover most of the energy which is normally lost in charging and discharging the load capacitor C_L. The load capacitor C_L is physically regarded as a capacitance made up by a plurality of pixel capacitors in a plasma display panel (see column 5, line 58-66).

Weber et al. teaches the usage of inductor (L) that is connected between the power source Vss and the plasma panel (see figure 5).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Yamaguchi et al., Tanaka, and Weber et al. to produce an integrated driver circuit that would allow for the address electrodes to not have to deliver the large sustain current to the discharging pixels, the address drivers will therefore have low current requirements. This in turn will allow lower cost drivers to be used.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. ***Claims 1-53*** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **claims 1-6** of U.S. Patent No. 6,111,555. Although the conflicting claims are not identical, they are not patentably distinct from each other. The subject matter claimed in **claims 1, 4-7, 11, 15, 18-20, 25, 28-30, 34-38, 41,47-51** of the instant application is fully disclosed in **claims 1-6** of the patent claiming the common subject matter as follows: a register capable of storing display bits each bit representing a next state for a corresponding electrode' a latch connected to the register having outputs, each output representing a current state for a corresponding electrode; logic circuits corresponding to the electrodes, each logic circuit generating a plurality of control signals based on the next state and the current state of the corresponding electrode; driver circuitry including a change up driver and a change down driver, each electrode being selectively connectable to the driver circuitry by the corresponding logic circuit control signals, wherein the logic circuits are configured such that the logic circuit control signals connect the change up driver to electrodes having a low current state and high next state and the change down driver to electrodes having a current state and low next state. Even though **claim 1** contains an additional limitation concerning a substantially

simultaneous connection of the driver to the electrodes, the claims of the instant application, as stated above, and the patent contain common patentable subject matter.

Claims 2-3, 10, 12-14, 16, 17, 21-24, 26, 27, 31-33, 39, 40, 42-46, and 52-53 are rejected for being dependent on a rejected base claim.

Allowable Subject Matter

6. ***Claims 10, 23, 35, 36, 48, and 49*** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Citation of Pertinent Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakamura (U.S. Patent No. 5,359,343) teaches a dynamic addressing display device includes a display panel and generates a number of dot data signals and data clock signals equal to the number of picture elements per row required to display one character on the display panel.

Scheffer et al. (U.S. Patent. No. 5,546,102) teaches an integrated driver circuitry including row and column signal generators.

Kaijimoto (U.S. Patent No. 5,864,328) teaches a driving method for LCD apparatuses that allows the dividing-driving method.

8. Any response to this action should be mailed to: Commissioner of Patents and Trademarks Washington, D.C. 20231; or faxed to (703)309-9051, (for formal communications intended for entry) or: (703)308-6606 (for informal or draft communications, please label "PROPOSED or DRAFT). Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive Arlington, VA., Sixth floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703)305-0143.

If attempts to reach the above examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703)305-9720.

DENNIS-DOON CHOW
PRIMARY EXAMINER

adn/ADN
June 17, 2001